**EXPT NO. DATE: - -**

**TRANSIENT RESPONSE OF NOR/NAND GATE**

**AIM**: To plot transient response of NOR/NAND Gate to Pulse Input

**RESOURCES:** NGSpice 28v software

**COURSE OUTCOMES:**

* ETC/ECE 5.5.3: Ability to understand and implement CMOS design and draw Euler’s diagram. Implement Spice for modelling CMOS design circuits.

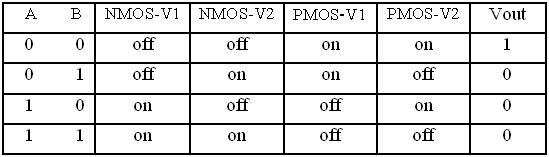
**OBJECTIVES:**

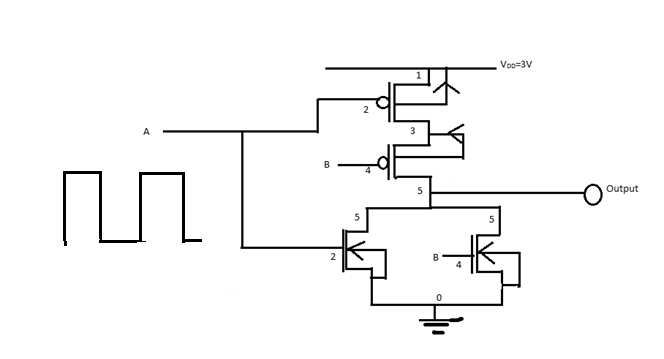
* To introduce NGSpice 28v compiler and in-built simulator

**THEORY:**

A)CMOS NOR Logic:

It can be constructed by using two parallel NMOS devices and two series PMOS transistor. A CMOS NOR gate circuit uses four MOSFETs just like the NAND gate, except that its transistors are differently arranged. Instead of two paralleled *sourcing* (upper) transistors connected to Vdd and two series-connected *sinking* (lower) transistors connected to ground, the NOR gate uses two series-connected sourcing transistors and two parallel-connected sinking transistors like this.The output is at logic 1 when all the inputs are low. For all other possible inputs, outputs is low or at logic 0.





**PROGRAM:**

\*Transient Response of nor gate to pulse input\*

.model mosn nmos vto=0.5

.model mosp pmos vto=-0.5

vdd 1 0 3

vin1 2 0 0

vin2 4 0 0

\*vin1 2 0 pulse(0 3 0ns .01ns .01ns 50ns 100ns)

\*vin2 4 0 pulse(0 3 0ns .01ns .01ns 100ns 200ns)

mn1 5 2 0 0 mosn

mn2 5 4 0 0 mosn

mp1 3 2 1 1 mosp

mp2 5 4 3 3 mosp

vin1 2 0 pulse (0 3 0 1ns 1ns 50ns 100ns)

vin2 4 0 pulse (0 3 0 1ns 1ns 50ns 200ns)

\*vin1 2 0 pulse(0 3 0ns .01ns .01ns 50ns 100ns)

\*vin2 4 0 pulse(0 3 0ns .01ns .01ns 100ns 200ns)

.tran 0ns 500ns 0.01ns

\*.tran 0ns 1000ns 0.01ns

.control

run

reset

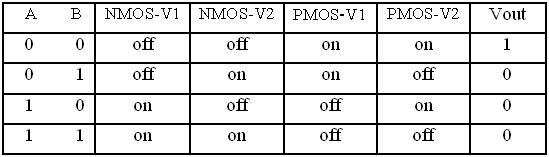
plot v(2) 4+v(4) 8+v(5)

.endc

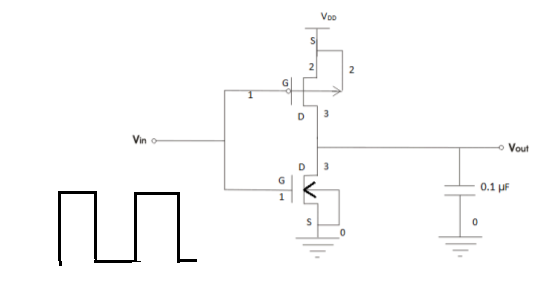
.end

**OUTPUT:**

**B) NAND Logic(pl edit logic according to NAND**

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**Nand CMOS design**

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\*To study the CMOS inverter and to observe the output response of pulse

.model mn1 nmos Vto=0.5

.model mp1 pmos Vto=-0.5

\*mos definition

m1 3 1 0 0 mn1

m2 3 1 2 2 mp1

\*energy to nmos and pmos

Vdd 2 0 3

Vgs 1 0 0

\*transient response response for pulse input

Vgs 1 0 pulse (0 3 0 1ns 1ns 50ns 100ns)

.tran 0ns 500ns 0.01ns

.control

run

reset

plot V(3) 4+V(1)

.endc

.end

**OUTPUT:**

**Conclusion:** The NOR gate using CMOS Structure was studied with a pulse wave and also inverter using a pulse wave was also studied and implemented using SPICE program.

**POST LAB QUESTIONS:**

1) 1. In negative logic convention, the Boolean Logic [1] is equivalent to:

a)+VDD  
b)0V  
c)-VDD  
d) None of the mentioned

Answer:b  
Explanation: In negative logic convention, the Boolean Logic [1] is equivalent to 0 V and Logic ‘0’ is equivalent to +VDD

2) In positive logic convention, the true state is represented as:

a) 1  
b) 0  
c) -1  
d) -0

Answer: a  
Explanation: In positive logic convention, the Boolean logic ‘1’ is known to be representing true state.

3) In CMOS logic circuit, the switching operation occurs because:  
a) Both n-MOSFET and p-MOSFET turns OFF simultaneously for input ‘0’ and turns ON simultaneously for input ‘1’  
b) Both n-MOSFET and p-MOSFET turns ON simultaneously for input ‘0’ and turns OFF simultaneously for input ‘1’  
c) N-MOSFET transistor turns ON, and p-MOSFET transistor turns OFF for input ‘1’ and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input ‘0’  
d) None of the mentioned

Answer:c  
Explanation: In CMOS logic circuit, the switching operation occurs because N-MOS transistor turns ON, and p-MOS transistor turns OFF for input ‘1’ and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input ‘0’. The networks are arranged such that one is ON and the other OFF for any input pattern.